on the substrate in
order to partition the wide and narrow substrate areas;
then, applies the high
density plasma chemical vapor deposition process to form an
oxide layer for
filling the said trenches and covering the surface on
silicon nitride layer;
then, selectively etching the part locating above the wide
substrate area or
employs a reverse tone mask pattern for simultaneously
etching the part of
oxide layer located above both the wide and narrow
substrate area until the
silicon nitride exposed; etch-backing the surface of oxide
in order to expose
the edge of silicon nitride; applies an isotropic etching
process for removing
silicon nitride layer and the oxide above it so as to
reserve the part in the
trench; Last, etching and removing the pad oxide layer to
accomplish the said
manufacturing process.

CHOSEN-DRAWING: Dwg.0/0

TITLE-TERMS:
MANUFACTURE METHOD SHALLOW TRENCH ISOLATE AREA
SEMICONDUCTOR COMPONENT CHEMICAL
MECHANICAL POLISH SUBSTRATE SIMPLIFY PROCESS INCREASE
CONTROL OXIDE LAYER THICK
ISOLATE AREA

DERWENT-CLASS: L03 U11

CPI-CODES: L04-C11C;

EPI-CODES: U11-C08A2;

SECONDARY-ACC-NO:
CPI Secondary Accession Numbers: C2001-100232
Non-CPI Secondary Accession Numbers: N2001-234682

DERWENT-ACC-NO: 2001-326550
DERWENT-WEEK: 200135

TITLE: Manufacturing method for shallow trench isolation area of semiconductor component - without the chemical mechanical polishing for substrate planarization to simplify the process and increase the control on oxide layer thickness of isolation area

INVENTOR: JANG, S

PATENT-ASSIGNEE: TAIWAN SEMICONDUCTOR MFG CO LTD[TASEN]

PRIORITY-DATA: 1998TW-0104235 (March 21, 1998)

PATENT-FAMILY:

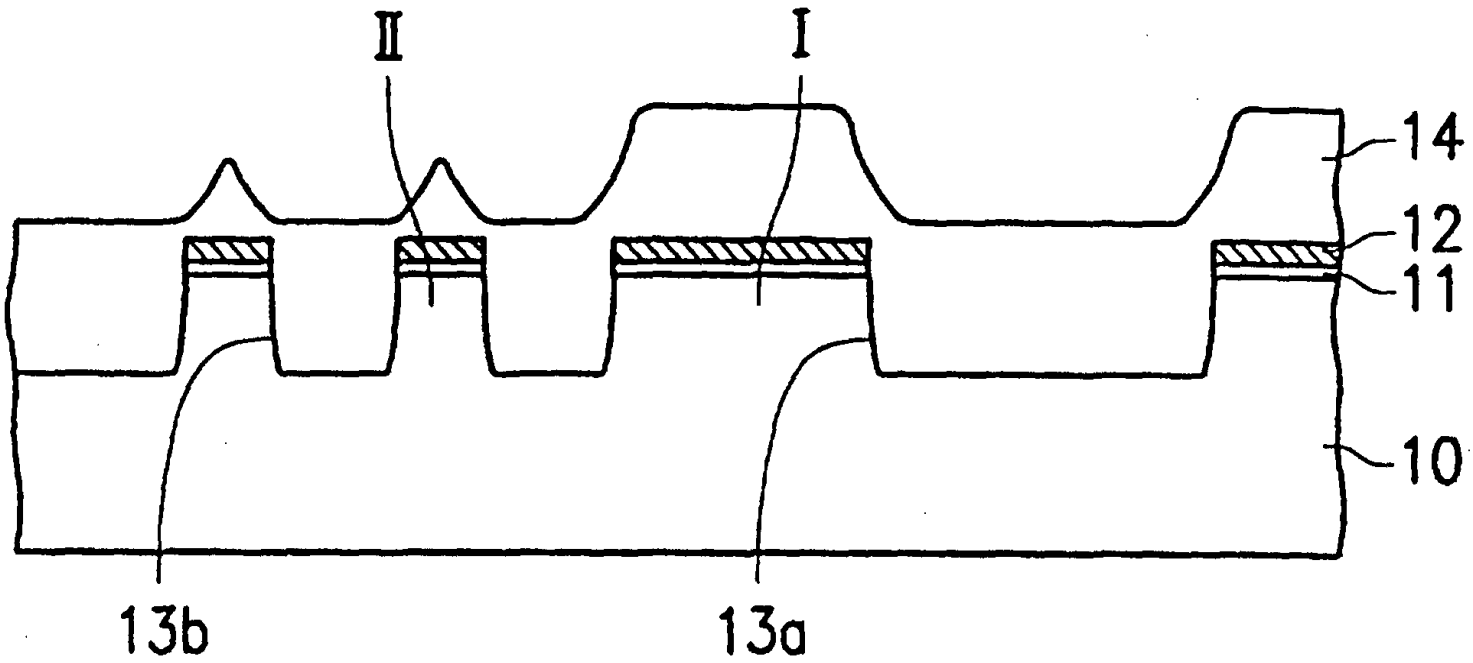
PUB-NO	PUB-DATE	LANGUAGE	PAGES	MAIN-IPC
TW 365051 A	July 21, 1999	N/A	001	H01L 021/76

APPLICATION-DATA:

PUB-NO	APPL-DESCRIPTOR	APPL-NO	APPL-DATE
TW 365051A	N/A	1998TW-0104235	March 21, 1998

INT-CL (IPC): H01L021/76

ABSTRACTED-PUB-NO: TW 365051A
BASIC-ABSTRACT: A kind of improved manufacturing method for shallow trench isolation area of semiconductor component with no need of chemical mechanical polishing for substrate planarization to simplify the manufacturing processes and reduce the production cost and increase the control on oxide layer thickness of isolation area. First, employs a pad oxide and silicon nitride layer as the mask for etching trenches of different pitches


II
I
14
12
11
10
13b
13a

formation of the
first oxide layer before the applying of PECVD for the uniformed thickness
formation of the second oxide layer that covered the surface of the first oxide
layer. Then comes a chemical mechanical polishing for the removal of the
protrusion from the oxide layer. The polishing shall stop as obtained while a
roughly flat surface is formed. Then, a dry or wet etching process would be
used to remove the portion of the height on the first and the second oxide
layer that is over the height of the silicon nitride layer, and the left part
in the trench can form the shallow trench isolation region.The uniform
thickness from the second oxide layer may increase the total thickness of the
oxide layers on the narrow substrate region and buffer the surface formation of
the oxide layer. Stopping the CMP processes once the planared surface is
formed, and followed by using the etching process to clean the oxide layer
which is higher than the silicon nitride layer, therefore, the sidewall of
silicon nitride layer would not be wounded and the undesired cavity would not
be created.

CHOSEN-DRAWING: Dwg.1a/3

TITLE-TERMS:
IMPROVE METHOD FORMING INTEGRATE CIRCUIT SHALLOW TRENCH ISOLATE REGION
COMBINATION HIGH DENSITY PLASMA CHEMICAL DEPOSIT

DERWENT-CLASS: L03 U11

CPI-CODES: L04-C01B;

EPI-CODES: U11-C08A2;

SECONDARY-ACC-NO:
CPI Secondary Accession Numbers: C2000-153200
Non-CPI Secondary Accession Numbers: N2000-379714

DERWENT-ACC-NO: 2000-513870
DERWENT-WEEK: 200047

TITLE: Improved method of forming integrated circuit shallow trench isolation
region by combining high density plasma chemical deposition

INVENTOR: CHEN, Y; JANG, S

PATENT-ASSIGNEE: TAIWAN SEMICONDUCTOR MFG CO LTD[TASEN]

PRIORITY-DATA: 1998TW-0112505 (July 29, 1998)

PATENT-FAMILY:

PUB-NO	PUB-DATE	LANGUAGE	PAGES	MAIN-IPC
TW 379411 A	January 11, 2000	N/A	019	H01L 021/76

APPLICATION-DATA:

PUB-NO	APPL-DESCRIPTOR	APPL-NO	APPL-DATE
TW 379411A	N/A	1998TW-0112505	July 29, 1998

INT-CL (IPC): H01L021/76

ABSTRACTED-PUB-NO: TW 379411A
BASIC-ABSTRACT: NOVELTY - The method includes using HDPCVD, for its optimal
trench filling capability, is ideal for making shallow trench isolation and
because of the topography of the oxide layer deposited during the planarisation
with the help of CMP, erosion would be created on the sidewall of the silicon
nitride layer in the narrow substrate region and unnecessary dishing in the
wider trench oxide layer. Therefore, the present invention provides an
improved method of forming integrated circuit shallow trench isolation region.
Using a high density plasma chemical gas deposition for the

CM P-FREE DISPOSABLE GATE PROCESS

This application claims priority under 35 USC § 119 (e) (1) of provisional application No. 60/054,299, filed Jul. 31, 1997.

BACKGROUND AND SUMMARY OF THE INVENTION

The present invention relates to integrated circuit structures and fabrication methods, and more specifically to forming an integrated circuit structure using a disposable gate process.

BACKGROUND: DISPOSABLE GATE PROCESS

A disposable gate process has been shown to provide a method by which a CMOS transistor structure can be scaled further into the sub-micron region while maintaining sufficiently low gate sheet resistance, small junction depth, and low junction capacitance. See provisional applications 60/029,215 filed Oct. 28, 1996 and 60/019,643 filed Oct. 28, 1996, which are hereby incorporated by reference.

A conventional disposable gate process is illustrated in FIGS. 2A–2C. FIG. 2A shows a field dielectric **114** which was blanket deposited over a disposable gate **120** (e.g. of silicon nitride) and pad oxide **122** which was formed over a semiconductor active area **102**. The field dielectric **114** is then chemically mechanically polished, leaving the surface of disposable gate **120** exposed as shown in FIG. 2B. In FIG. 2C disposable gate **120** has been removed (e.g. by a hot phosphoric acid). A gate electrode can now be deposited in the space **115** left by the removal of disposable gate **120**.

The chemical mechanical polishing step (CMP) in the conventional process discussed above is a polishing technique which provides global planarization. However, CMP can be a problematic step in this conventional process because of the polish rate dependence on gate density. Yota et al., *Integration of ICP High-Density Plasnia CVD with CMP and Its Effects on Planarity for Sub-0.5 μm CMOS Technology*, 2875 Proceedings of the SPIE 265 (1997), which is hereby incorporated by reference. The CMP process is difficult to control because of the pattern sensitivity of the polish rate.

Background: HDP-CVD

The basic HDP-CVD (high density plasma-chemical vapor deposition) process involves a simultaneous deposition and etch component and is already well-established in the semiconductor industry. HDP-CVD can provide very non-conformal deposition, in which material buildup occurs almost complete on the flat surfaces of the starting structure, and not on sidewalls. See e.g., A. Chatterjee et al., *A Shallow Trench Isolation Study for 0.25/0.18 μm CMOS Technologies and Beyond*, 156 Symposium on VLSI Technology Digest (1996); S. Nag et al., *Comparative Evaluation of Gap-Fill Dielectrics in Shallow Trench Isolation for Sub-0.25 μm Technologies*, 841 IEDM (1996), which are hereby incorporated by reference.

CMP-Free Disposable Gate Process

The present application solves the problem of polish rate dependence on gate pattern density by using a highly non-conformal field dielectric to leave the disposable gate partially exposed, thereby eliminating the need to chemically-mechanically-polish the field dielectric to expose the disposable gate. In a sample embodiment, HDP-CVD oxide is deposited non-conformally as the field oxide over a disposable gate structure. The deposition process uses a sputter component to achieve minimal deposition on the sidewalls of the disposable gate. The oxide deposition is preferably stopped before the oxide filling up the trench and the oxide depositing on top of the disposable gate meet, thus leaving the sidewalls of the disposable gate partially exposed. Optionally, a short oxide etch can be used to selectively remove any oxide which deposited on the sides of the disposable gate, thereby leaving the sidewalls of the gate partially exposed. Because the sidewalls are exposed, the process can proceed directly to selective removal of the disposable gate, rather than going through a CMP step to expose the disposable gate before removal can proceed.

Advantages of the disclosed methods and structures include:

- eliminating the need for CMP after field-oxide deposition;
- simplifying the overall disposable gate process;
- eliminating pattern sensitivity to the degree of planarity;
- high-k gate dielectrics and/or metal gates (e.g. aluminum) are not subjected to high temperatures in a disposable gate process;
- limits on lateral dimensions of a disposable gate can be avoided;
- a thicker disposable gate structure can be used to provide a higher margin of error;
- the field oxide can provide a thicker oxide etch-stop than the gate oxide.

BRIEF DESCRIPTION OF THE DRAWING

The disclosed inventions will be described with reference to the accompanying drawings, which show important sample embodiments of the invention and which are incorporated in the specification hereof by reference, wherein:

FIG. **1** shows a sample CMP-free process flow for formation of a disposable gate structure.

FIGS. **2A–2C** illustrate a previously known step in the process.

FIGS. **3A–3E** are cross-sectional diagrams of a structure formed according to a preferred embodiment of the invention during various stages of fabrication.

FIG. **4** is a cross-sectional diagram of a structure formed according to an alternative embodiment of the invention during various stages of fabrication.

FIGS. **5A–5E** are cross-sectional diagrams of a structure formed according to an alternative embodiment of the invention during various stages of fabrication.

Corresponding numerals and symbols in the different figures refer to corresponding parts unless otherwise indicated.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

The numerous innovative teachings of the present application will be described with particular reference to the presently preferred embodiment. However, it should be understood that this class of embodiments provides only a few examples of the many advantageous uses of the innovative teachings herein. In general, statements made in the specification of the present application do not necessarily delimit any of the various claimed inventions. Moreover, some statements may apply to some inventive features but not to others.

Overview of a CMP-Free Disposable Gate Process

FIG. **1** shows a sample CMP-free process flow for forming a disposable gate structure. Those of ordinary skill in the